COMPACT SRAM CELL LAYOUT FOR IMPLEMENTING ONE-PORT OR TWO-PORT OPERATION

Abstract of the Disclosure

Compact static random access memory (SRAM) cell layouts are provided for implementing one-port and two-port operation. The SRAM cell layouts include a plurality of field effect transistors (FETs). The plurality of FETs defines a storage cell and a pair of wordline FETs coupled to the storage cell. Each of the plurality of FETs has a device structure extending in a single direction. The device structure of each of the plurality of FETs includes a diffusion layer, a polysilicon layer and first metal layer. A local interconnect connects the diffusion layer, the polysilicon layer and the first metal layer. Each of the pair of wordline FETs having a gate input connected to a wordline. The wordline including a single wordline for implementing one-port operation or two separate wordline connections for implementing two-port operation. The local interconnect includes a metal local interconnect that lays on the diffusion and polysilicon layers for electrically connecting diffusion and polysilicon layers and a metal contact that extends between the metal local interconnect and the first level metal for electrically connecting diffusion and polysilicon layers and the first level metal. Alternatively, a metal contact lays directly on the diffusion and polysilicon layers electrically connecting diffusion and polysilicon layers and the first level metal. The local interconnect further includes a conduction layer disposed on a butted diffusion connection of diffusion-p type and diffusion-n type and a metal local interconnect disposed on the conduction layer.